REMARKS

Claims 1-10 are all the claims pending in the application. By this Amendment, Applicant editorially amends claims 1 and 3-7 to cure minor informalities. In addition, claim 1 is amended to further clarify the invention.

I. Preliminary Matters

As preliminary matters, the Examiner has acknowledged Applicant's claim to foreign priority and has indicated receipt of the certified copy of the priority document. Also, the Examiner has returned the initialed form PTO/SB/08 submitted with the Information Disclosure Statement filed on October 15, 2004.

II. Summary of the Office Action

The Examiner objected to the drawings and claim 6. In addition, the Examiner rejected claims 7-10 under 35 U.S.C. § 112, claims 1 and 2 under 35 U.S.C. § 102, and claims 3-5 under 35 U.S.C. § 103.

III. Objection to the Drawings

The Examiner has objected to the drawings filed on November 16, 2001. Specifically, the Examiner alleges that a) FIGS. 1, 2, and 4 need more descriptive labels for the depicted elements, b) labels FIGS. 3 and 4 are handwritten, and c) the drawings fail to show every feature of the invention specified in the claims.

Applicant is submitting herewith four (4) sheets of replacement drawings. The submitted drawings are believed to obviate the Examiner's objection. That is, in accordance with MPEP §

608.02, Applicant labels all boxes with more descriptive labels. Accordingly, Applicant respectfully requests the Examiner to withdraw these objections to the drawings.

Applicant further respectfully notes that there is no requirement to provide descriptive labels for the signals. Abbreviations are commonly used for illustrating signals. If the Examiner decides to maintain this objection to the drawings, requiring that Applicant labels the signals such as IT in FIG. 1, Applicant respectfully requests the Examiner to provide supporting passages from the MPEP that would require descriptive labeling of the signals.

Also, the Examiner alleges that certain elements set forth in the claims are not depicted in the drawings. Specifically, the Examiner alleges that signaling bytes claimed in claim 6 are not depicted in the Drawings (*see* page 2 of the Office Action). Applicant respectfully submits that an exemplary signaling byte is depicted in Table 7.

Moreover, the Examiner alleges that elements MSA of claim 9 and element MS of claim 10 are not depicted in the Figures (*see* page 2 of the Office Action). Applicant respectfully directs the Examiner's attention to the replacement sheet of Fig. 2, where the MSA is an exemplary input memory block and the MS is an exemplary state machine.

In view thereof, Applicant respectfully requests the Examiner to indicate acceptance of the Drawings.

IV. Claim Objection

The Examiner objected to claim 6 because of minor informalities. Applicant respectfully requests the Examiner to withdraw this objection in view of the self-explanatory claim amendments being made herein.

V. Claim Rejection under § 112

Claims 7-10 are rejected under 35 U.S.C. § 112, second paragraph. It is appropriate and necessary for the Examiner to withdraw this rejection in view of the self-explanatory claim amendment being made herein.

Moreover, Applicant respectfully submits that an antecedent basis problem should not have precluded the Examiner from examining claims 7-10 on the merits. MPEP § 2173.06 recites:

> When terms of a claim are considered to be indefinite, at least two approaches to the examination of an indefinite claim relative to the prior art are possible.
>
> First, where the degree of uncertainty is not great, and where the claim is subject to more than one interpretation and at least one interpretation would render the claim unpatentable over the prior art, an appropriate course of action would be for the examiner to enter two rejections: (A) a rejection based on indefiniteness under 35 U.S.C. § 112, second paragraph; and (B) a rejection over the prior art based on the interpretation of the claims which renders the prior art applicable. See, e.g., *Ex parte Ionescu*, 222 USPQ 537 (Bd. App. 1984). When making a rejection over prior art in these circumstances, it is important for the examiner to point out how the claim is being interpreted. Second, **where there is a great deal of confusion and uncertainty as to the proper interpretation of the limitations of a claim**... (emphasis added)
>
> **The first approach is recommended from an examination standpoint because it avoids piecemeal examination** in the event that the examiner's 35 U.S.C. § 112, second paragraph

> rejection is not affirmed, and may give applicant a better appreciation for relevant prior art if the claims are redrafted to avoid the 35 U.S.C. § 112, second paragraph rejection, (emphasis added).

Clearly, a simple antecedent basis problem does not create a great deal of confusion and uncertainty as to avoid interpreting the claims for the purpose of examination on the merits. Accordingly, Applicant respectfully submits that the Examiner should have considered claims 7-10 on their merits.

VI. Rejection under 35 U.S.C. § 102(b)

Claims 1 and 2 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,278,836 to Iimura et al. (hereinafter "Iimura"). Applicant respectfully traverses this rejection in view of the following comments.

Of these rejected claims, only claim 1 is independent. Claim 1 recites:

> at least a central board having an active or inactive state; and
>
> one or more input/output peripheral boards for exchanging data frames and control bytes over a connection between a peripheral board and a central board,
>
> wherein said data frames contain said control bytes, comprising at least one of bytes indicating frame alignment, bytes indicating synchronization, and bytes monitoring the connection and switching of the state of said central board, and
>
> wherein said data frames are bitwise converted before being exchanged between the peripheral boards and the central board.

The Examiner alleges that claim 1 is directed to an interface system and is anticipated by Iimura. Specifically, the Examiner alleges that Iimimura's disclosure of a frame with a control field and

converting serial data to into parallel data and vise versa is equivalent to the data frame containing control bytes and converting the data frame bitwise prior to exchange, as set forth in claim 1. Applicant respectfully disagrees. Applicant has carefully studied Iimura's discussion of the frames and data conversion and Applicant respectfully submits that Iimura's frame lacks having control bytes and especially control bytes for one or more of the following: frame alignment, synchronization, and monitoring the connection and switching of the active board and exchanging frames between the boards. In addition, Applicant respectfully submits that Iimura fails to disclose a bitwise conversion.

To be an "anticipation" rejection under 35 U.S.C. § 102, the reference must teach every element and recitation of the Applicant's claims. Rejections under 35 U.S.C. § 102 are proper only when the claimed subject matter is identically disclosed or described in the prior art. Thus, the reference must clearly and unequivocally disclose every element and recitation of the claimed invention.

Iimura discloses a multichannel communication processing system having line control apparatus means for analyzing receiving frames and channel-controlling transmitting frames, a DMA control apparatus for transferring the data not via a host processor but directly to a main memory, a memory for storing a variety of data and a communication protocol processing program, a CPU for controlling the communication processing system as a whole and a line correspondence apparatus including line correspondence units provided between the lines and the line control apparatus whereby serial interfaces with channels of the plurality of lines are

effected (*see* Abstract). In Iimura, a frame has an address, a control field, an information field, and a frame check sequence interposed between flag sequences (col. 4, lines 61 to 66).

Iimura further discloses the line correspondence unit 61 that includes 8-bit receiving shift register 64 for converting serial receiving data into parallel receiving data, a receiving FIFO memory 62 for temporarily accumulating the data, a transmitting FIFO memory 63 for temporarily accumulating the transmitting data, and a transmitting shift register 65 for converting the parallel transmitting data into the serial transmitting data. Iimura discloses that at the receiving time, the serial data received at a rate of, e.g., 16 kbps are converted 8-bitwise into parallel data by the receiving shift register 64 (emphasis added). The parallel data are then stored in a receiving FIFO memory 62. The line correspondence unit 61 transmits a signal indicating, for example, [existence of receiving FIFO memory data] to the line control circuit 8. The same unit 61 then waits for processing by the line control circuit 8. The line control circuit 8 sequentially reads the data of the receiving FIFO memory 62 at timings when processing the receiving data of the line correspondence unit of that channel. The circuit 8 then executes the necessary process (Fig. 6; col. 6, line 55 to col. 7, line 11).

Iimura, however, fails to teach or suggest exchanging frames with control bytes between the line control circuit 8 (alleged central board) and the line correspondence unit 61 (alleged peripheral boards). That is, in Iimura, the received frame is taken apart in the correspondence unit 61. That is, the line control circuit 8 receives a signal informing the receipt of frames coming in from the plurality of lines corresponding to units 61-68, which in turns informs the CPU and the CPU reads the control information (col. 5, lines 4 to 27). Then, the information

fields of the frames, accumulated in the line control circuit 8, are transferred while being marked with the channel numbers via the receiving data bus 13 to the DMA control circuit 9 (col. 5, lines 28 to 33). In other words, Iimura fails to teach or suggest exchanging frames between the control circuit unit 8 and the correspondence units 61-68.

Moreover, Iimura only discloses a frame having a control field and fails to teach or suggest a frame having control bytes. Finally, in Iimura, there is no teaching or suggest of the control bytes being one or more of bytes for frame alignment, synchronization bytes, and bytes for monitoring the connection and switching of the active board. Since Iimura only teaches having a control field and fails to teach the control bytes for alignment, synchronization, and/or monitoring the connection, the rejection is improper as it lacks "sufficient specificity" required under 102. "[A]nticipation under § 102 can be found only when the reference discloses exactly what is claimed and that where there are differences between the reference disclosure and the claim, the rejection must be based on § 103 which takes differences into account." *Titanium Metals Corp. v. Banner*, 778 F.2d 775, 227 USPQ 773 (Fed. Cir. 1985); MPEP § 2131.

Therefore, "at least a central board having an active or inactive state; and wherein said data frames contain said control bytes, comprising at least one of bytes indicating frame alignment, bytes indicating synchronization, and bytes monitoring the connection and switching of the state of said central board, and wherein said data frames are bitwise converted before being exchanged between the peripheral boards and the central board," as set forth in claim 1 is not disclosed by Iimura, which lacks exchanging frames with control bytes between the line correspondence units 61-68 and the line control circuit 8 and which also lacks having the control

field include alignment, synchronization, and/or monitoring the connectiong and switching of the state of the active board. For at least these exemplary reasons, Applicant respectfully submits that claim 1 is patentable over Iimura. Accordingly, Applicant respectfully requests the Examiner to withdraw this rejection of claim 1 and its dependent claim 2.

Rejection under 35 U.S.C. § 103(a)

Claims 3-6 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Iimura. Applicant respectfully traverses this rejection in view of the following comments. Applicant has already demonstrated that Iimura fails to teach or suggest all of the unique features of claim 1. Accordingly, claims 3-6 may be patentable at least by virtue of their dependency on claim 1.

Moreover, Iimura only discloses a frame having a frame check sequence, flag sequences, and having an address. Iimura, however, fails to teach or suggest the frame check sequence, the flag sequences, and the address being an indication of a frame alignment, synchronization, and the monitoring of the connection, respectively. For example, an address clearly does not monitor the connection. Data may be sent at a particular address of a destination. The data, however, may never reach the destination if the destination is not connected. In short, in Iimura, there is no teaching or suggestion of the frame check sequences, flag sequences, and an address designating the frame alignment, synchronization, and the monitoring of the connection.

The Examiner further alleges that it would have been obvious to super-size the frame (*see* page 5 of the Office Action). Applicant respectfully submits, however, that from the tenor of these grounds of rejection, it would appear that the Examiner has decided that the present invention is too simple to be deserving of a patent. As a result, the Examiner has formulated grounds of

rejection which, at first blush, appear to be based on actual prior art disclosure, but instead are based on a hindsight rationale that anyone with of a frame having a control field could, in theory, have implemented the claimed interface system.

However, MPEP § 2141 states that "Office policy has consistently been to follow Graham v. John Deere Co. in the consideration and determination of obviousness under 35 U.S.C. § 103." Grounds of rejection based on a rationale such as the one just described distort each of the Graham factual inquiries, and produce a distorted determination as a result. **Since the rationale is not rooted in actual prior art**, productive discussion regarding the true scope and content of the prior art is no longer feasible. This, in turn, renders it impossible to clearly ascertain the actual differences between the prior art and the claims at issue. Also, since the rationale is a purely hypothetical construct, it is by its very nature a creature of hindsight, which makes any advance over the art appear trivial. If the Examiner alleges that super-sizing a frame of one byte into a number of bytes and transmitting this super-sized frame between a central board and a peripheral board is obvious, Applicant respectfully requests the Examiner to cite an appropriate reference or references, as well as to provide motivation for combining these references with Iimura.

Claim 6 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Iimura in view of U.S. Patent No. 6,603,776 to Fedders et al. (hereinafter "Fedders"). Applicant respectfully traverses this rejection in view of the following comments. Claim 6 depends on claim 1. Applicant has already demonstrated that Iimura does not teach or suggest all of the unique features of claim 1. Fedders is only cited for its teachings of mapping (*see* page 5 of the Office

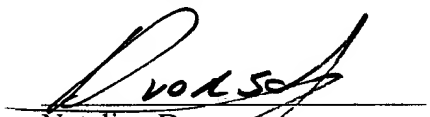
Action) and as such clearly fails to cure the deficient teachings of Iimura. Accordingly, claim 6 is patentable at least by virtue of its dependency on claim 1.

Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly invited to contact the undersigned attorney at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



SUGHRUE MION, PLLC
Telephone: (202) 293-7060
Facsimile: (202) 293-7860

WASHINGTON OFFICE
23373
CUSTOMER NUMBER

Nataliya Dvorson
Registration No. 56,616

Date: November 14, 2005

Attorney Docket No.: Q67311

AMENDMENTS TO THE DRAWINGS

Figure legends have been added to Figures 1, 2, and 4, for all boxes are labeled.

In Figures 3 and 4 handwritten labels are replaced with formal labels.

Attachment: Four (4) Replacement Sheets